

عنوان مقاله:

An Efficient Hardware Implementation for H.264 Binary Arithmetic Encoder

محل انتشار:

چهاردهمین کنفرانس بین المللی سالانه انجمن کامپیوتر ایران (سال: 1388)

تعداد صفحات اصل مقاله: 5

نویسندگان:

Farzad Zargari - *Multimedia Systems Research Group, IT Research Institute, Iran Telecom Research Center, Tehran, Iran*

Ehsan Azimi - *Multimedia Systems Research Group, IT Research Institute, Iran Telecom Research Center, Tehran, Iran*

خلاصه مقاله:

Binary Arithmetic Coding (BAC) is among the techniques used in H.264 video coding standard to improve the coding efficiency. BAC includes an iterative process of renormalization with up to seven iterations for coding each symbol. Since BAC is also a computational intensive unit in H.264 encoder, various hardware realizations have been proposed for it in the literature. In this paper, we propose a hardware implementation for BAC, which uses lookup table to avoid the iterative coding process and achieves coding rate of one symbol per clock at 260 MHz clock rate. Post synthesise simulation results indicate that the proposed architecture is a resource and speed efficient hardware .for H.264 binary arithmetic encoder

کلمات کلیدی:

لینک ثابت مقاله در پایگاه سیویلیکا:

<https://civilica.com/doc/72995>

