

عنوان مقاله:

Improving Accuracy, Area and Speed of Approximate Floating- Point Multiplication Using Carry Prediction

محل انتشار:

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خلاصه مقاله:

Arithmetic units are essential in digital circuit construction, and the enhancement of their operation would optimize the whole digital system. Among them, multipliers are the most important operational units and are used in a wide range of digital systems such as telecommunication signal processing, embedded systems, and mobile technology. The main drawback to a multiplication unit is its high computational load, which leads to considerable power consumption and an increased area of silicon. This also reduces the speed, which negatively affects the digital host functionality. Estimating arithmetic is a new branch of computer arithmetic implemented by discarding or manipulating a portion of arithmetic circuits and/or intermediate computations. Applying estimated arithmetic in arithmetic units would improve the speed, power consumption, and the implementation area by sacrificing a slight amount of result accuracy. This article develops and analyzes an estimated truncated floating-point multiplier for single precision operands that is capable of compensating for errors to a desired level by applying the least significant columns of the partial product matrix. These errors are caused by removing a number of carry digits in the partial product matrix which make a direct contribution to rounding the floating-point numbers. The evaluation results indicate that the proposed method improves speed, accuracy, and silicon area, in comparison with common truncated multiplication methods.

کلمات کلیدی:

estimated arithmetic; partial product matrix; rounding; truncated multiplier; error correction

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